UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,242	01/25/2001	Melissa D. Cooper	95-360	3543

20736 7590 12/02/2004

MANELLI DENISON & SELTER
2000 M STREET NW SUITE 700
WASHINGTON, DC 20036-3307

EXAMINER	
TON, ANTHONY T	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,242	COOPER, MELISSA D.	
	Examiner	Art Unit	
	Anthony T Ton	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☒ Claim(s) *12-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/17/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

PHIRIN SAM
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETALED ACTIONS

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1, 6, 7** and **11** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Tateishi* (US Patent No. 5,383,177) in view of *Payne et al.* (US Patent No. 6,347,395) hereinafter referred to as *Payne.*

a) **In Regarding to Claim 1**: *Tateishi* disclosed a method for testing a packet switching device *(see col.1 lines 6-13)* having an expansion port configured for transferring data according to a prescribed protocol, the method comprising:

receiving by an external logic unit an expansion port frame from the expansion port via an expansion bus *(see Fig.1: block 1a (external logic unit); col.9 lines 34-40 (expansion port frame); in Fig.1, wherein the position at Output Highway Data that connected to OWi - OWn (expansion bus) is considered as an expansion port of the device under test at the block 6)*;

generating by the external logic unit a new expansion port frame based on reception of the expansion port frame *(see col.11 line 30-31: the packet section 21 generates the packet data);* and

outputting the new expansion port frame onto the expansion bus for reception by the expansion port of the packet switching device *(see col.11 lines 31-33: The packet data are transferred to one input highway IW1 (expansion bus)).*

Tateishi failed to explicitly disclose **a network switch chip** to be tested as a claimed subject matter of the Applicants.

Payne disclosed such a network switch chip *(seeFig.3-2: block 310)*

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such a network switch chip, as taught by *Payne* with *Tateishi*, so that any integrated circuit can be tested by using the testing apparatus of *Tateishi*. The motivation for doing so would have been to overcome a cost in testing complex custom chip designs *(see Payne: col.1 line 39 – col.2 line 4)*. Therefore, it would have been obvious to combine *Payne* with *Tateishi* in the invention as specified in the claim.

b) **In Regarding to Claim 7**: the claimed subject matters of this claim are the same as that of claim 1. Therefore, the rejections to the claim 1 would apply to reject this claim, in a test system as taught.

c) **In Regarding to Claims 6** and **11**: *Tateishi* disclosed all aspects of these claims as set forth in claims 1 and 7, respectively.

Tateishi failed to explicitly disclose the external logic unit is implemented using a field programmable gate array.

Payne disclosed such an external logic unit is implemented using a field programmable gate array *(see Fig.3-1: block 232 FPGA)*.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such an external logic unit is implemented using a field programmable gate array, as taught by *Payne* with *Tateishi*, so that a plurality of integrated circuits (IC), which are implemented into a bigger IC such as a FPGA, can be tested with the testing apparatus of

Tateishi. The motivation for doing so would have been to provide internal signals on a block under test can be easily be inspected by simply routing those signals to pins on the FPGA *(see Payne: col.6 lines 55-58)*. Therefore, it would have been obvious to combine *Payne* with *Tateishi* in the invention as specified in the claims.

3. **Claims 2-5** and **8-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Tateishi* (US Patent No. 5,383,177) in view of *Payne et al.* (US Patent No. 6,347,395) as applied to claims 1, 6, 7 and 11 above, and further in view of *Fowler et al.* (US Patent No. 5,721,728) hereinafter referred to as *Fowler*.

a) **In Regarding to Claim 8**: *Tateishi* disclosed all aspects of this claim as set forth in claim 7.

Tateishi failed to explicitly disclose the external logic unit is configured for generating the new expansion port frame by changing data within the received expansion port frame.

Fowler disclosed such a changing data within the received expansion port frame *(see col.5 lines 53-59: The application layer 14c the generates a second user portion based on the test parameters)*.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such a changing data within the received expansion port frame, as taught by *Fowler* with *Tateishi*, so that frames can be used in different purposes. The motivation for doing so would have been to provide a second user portion having a data structure that may comprise a second user portion of a test message *(see Fowler: col.5 line 65 – col.6 line 2)*. Therefore, it

would have been obvious to combine *Fowler* with *Tateishi* in the invention as specified in the claim.

b) **In Regarding to Claim 9**: *Tateishi* disclosed all aspects of this claim as set forth in claims 7 and 8.

Tateishi failed to explicitly disclose the external logic unit is configured for changing data by parsing a header of the expansion port frame to retrieve a source address value from a source address field and a destination address value from a destination address field, the external logic unit inserting the source address value into the destination address field, and the destination address value into the source address field, of the new expansion port frame.

However, *Fowler* disclosed a called party field and a calling party field corresponding to a called party address and calling party address, respectively. When generating a new data (ph-ph packet), application processor uses the corresponding data in the ph-ph packet to generate the called party field and the calling party field as illustrated in Fig.2; wherein the called party field is set equal to the called party address block of test parameters as shown in Fig.3, and the calling party field is set equal to the original called party information passed within the ph-ph packet *(see col.10 lines 10-24)*. Therefore, it would be obvious that *Fowler* disclosed such the claimed subject matters of the instant claim.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such claimed subject matters of the instant claims to the packet, as taught by *Fowler* with *Tateishi*, so that a desired packet can be generated without creating a new data for the packet header of the packet. The motivation for doing so would have been to provide suitable facilities for adequately testing the segmentation and reassembly functionality of signal

connection control parts and an application layer *(see Fowler: col.2 lines 1-9)*. Therefore, it would have been obvious to combine *Fowler* with *Tateishi* in the invention as specified in the claim.

c) **In Regarding to Claim 10**: Tateishi disclosed all aspects of this claim as set forth in claims 7-9.

Tateishi failed to explicitly disclose the external logic unit is configured for inserting a new device identifier value into a device identifier field in the new expansion port frame.

Fowler disclosed such inserting a new device identifier value into a device identifier field in the new expansion port frame *(see col.4 lines 61-63: PH Number Byte 53 contains a value that identifies the second protocol handler 14)*.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such inserting a new device identifier value into a device identifier field in the new expansion port frame, as taught by *Fowler* with *Tateishi*, so that a desired packet header can be generated without creating a new data for the packet header. The motivation for doing so would have been to provision time efficiency and avoid error when creating a new data. Therefore, it would have been obvious to combine *Fowler* with *Tateishi* in the invention as specified in the claim.

d) **In Regarding to Claims 2-4**: these claims are rejected for the same reasons as claims 8-10, respectively because the apparatus in claims 8-10 can be used to practice the method steps of claims 2-4, respectively.

e) **In Regarding to Claim 5**: *Tateishi* disclosed all aspects of this claim as set forth in claims 1-4.

Tateishi failed to explicitly disclose the external logic unit is implemented using a field programmable gate array.

Payne disclosed such an external logic unit is implemented using a field programmable gate array *(see Fig.3-1: block 232 FPGA).*

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such an external logic unit is implemented using a field programmable gate array, as taught by *Payne* with *Tateishi*, so that a plurality of integrated circuits (IC), which are implemented into a bigger IC such as a FPGA, can be tested with the testing apparatus of *Tateishi*. The motivation for doing so would have been to provide internal signals on a block under test can be easily be inspected by simply routing those signals to pins on the FPGA *(see Payne: col.6 lines 55-58).* Therefore, it would have been obvious to combine *Payne* with *Tateishi* in the invention as specified in the claim.

Allowable Subject Matter

4. **Claims 12-19** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Remarks

5. Applicant's arguments filed on August 17, 2004, wherein claim 7 is amended and claims 12-19 are added, have been fully considered but they are not persuasive.

6. Claims 1, 6, 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Tateishi* (US Patent No. 5,383,177) in view of *Payne et al.* (US Patent No. 6,347,395).

Although each of the independent claims 1 and 7 specifies testing a network switch chip, *Tateishi* specifies testing a packet switching device namely the under-test device 6 *(see col.1 lines 6-13 and Fig.1)*. This is a principle subject matter of *Tateishi* that differed from the Applicant's instant claims. However, *Payne* disclosed such a network switch chip *(seeFig.3-2: block 310)*. Please see the motivation in the section 2 above.

In the previous Office Action, Examiner had an interpretation in a different way relating to the external logic unit and expansion port; such an interpretation is not very suitable as that of the instant claims. In this Office Action, Examiner considers the packet switching testing apparatus and under-test device of *Tateishi* as the external logic unit and network switch chip of the instant claims, respectively.

With the claimed subject matter of generating by the external logic unit a new expansion port frame based on reception of the expansion port frame. Based on the control information adding section 27 and control information determining section 37 in Fig.11 and that of a flow chart shown in Fig.12, a new expansion port frame is generated based on reception of the expansion port frame because if a disposed packet received by the receiving section of the packet switching testing apparatus with a disposal flag sets to "1" *(i.e. fail) (see Fig.12 steps 507 and 508)*, the transmitting section of the packet switching testing apparatus will have to re-initialize or reset the disposal flag in a new packet for a next test *(see col.11 line 60-col.12 line 34)*.

Furthermore, Examiner respectfully disagrees with the Applicants that *Tateishi* neither discloses nor suggests and an expansion port or an expansion bus. In fact, *Tateishi* does disclose

an expansion bus as the instant claims *(see Fig.1: bus OWi - OWn of the device under test at the block 6, which would be considered as the expansion bus of the instant claims).*

With the disclosures of *Tateishi*, all claimed subject matters of the claims 1 and 7 have been disclosed by *Tateishi,* **except for** a tested network switch chip that was described above; and therefore, the rejection to the claims 1 and 7 is still maintained.

Claims 2-5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Tateishi* (US Patent No. 5,383,177) in view of *Payne et al.* (US Patent No. 6,347,395) as applied to claims 1, 6, 7 and 11 above, and further in view of *Fowler et al.* (US Patent No. 5,721,728).

This rejection is respectfully traversed and considered. However, the rejection is still maintained as the reasons that have been described in section 3 above.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Anthony T Ton** whose telephone number is **571-272-3076**. The examiner can normally be reached on M-F: 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ken Vanderpuye** can be reached on **571-272-3078**. The fax phone number for the organization where this application or proceeding is assigned is **703-872-9306**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Respectfully submitted,

by :
Anthony T. Ton
Patent Examiner
November 15, 2004

PHIRIN SAM
PRIMARY EXAMINER